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65913	7590	02/27/2008	EXAMINER	
NXP, B.V.			KNOLL, CLIFFORD H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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ip.department.us@nxp.com

Response to Arguments

Applicant's arguments filed 1/7/08 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Yoshida fails to literally employ the explicit phrase "special function registers", and thus fails to disclose the claimed "special function registers" (p. 6); however, at the cited passage, it is seen that Yoshida teaches the use of registers to perform special functions, namely that of addend, thus distinguishing them from general registers, likewise, the result register which also acquires a special function thereby. Examiner maintains these special functions employed at the cited passage are adequate to anticipate the claimed "special function registers"; if the Applicant intends special functions that are distinct from those designated by Yoshida, then these special functions must be positively recited.

Applicant further argues that the combination is improper because Applicant is unable to ascertain what the "alleged modification of Mitsuhira involves" (p. 7). Examiner maintains that Mitsuhira discloses registers; however there is no discussion in Mitsuhira regarding the use of the registers for special functions. Yoshida teaches that registers, a basic component of a computer, can be used in a certain way, that is they may have a particular function, even more particularly, they may have these particular functions during the execution of arithmetic operations. In an arithmetic operation, the functions of addends and sum are special and thus Yoshida anticipates these recited limitations of the registers that Mitsuhira neglects to mention.

Regarding claim 8, Applicant argues that the combination fails to teach "register block selection data indicative of a pre interrupt switch state"; however this is taught by Fujimura who shows that as is commonly known, an interrupt interrupts something. Fujimura teaches explicitly that this is the case, and that furthermore, this pre existing state is restored after the interrupt. A person of ordinary skill in the art would be motivated to use Fujimura to return to a pre existing state in order that the task being performed prior to the interrupt may be resumed; this is a fundamental nature of what an interrupt is: "the suspension of a process to handle an event external to the process" (*The Authoritative Dictionary of IEEE Standard Terms 7th Edition, 2000*). Thus a pre existing state is not only explicitly noted by Fujimura, but it is an essential aspect of what constitutes an interrupt.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Clifford H Knoll/
Clifford H Knoll
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